

Claims

What is claimed is:

1. An apparatus comprising:

an integrated circuit die comprising an internal signal pad arranged at a location away
5 from a periphery of the die, a peripheral signal pad arranged proximate the periphery of the die, and
a switch coupled between the internal signal pad and the peripheral signal pad;

the switch being configurable in at least a first state in which the internal signal pad
is not operatively connected to the peripheral signal pad, and a second state in which the internal
signal pad is operatively connected to the peripheral signal pad;

10 the switch being configurable in one of the first and second states responsive to a
control signal having one of first and second signal characteristics, respectively;

wherein the switch is configured in the first state during normal operation of the
integrated circuit die; and

wherein the switch is configured in the second state to permit test access to the
15 internal signal pad via the peripheral signal pad.

2. The apparatus of claim 1 wherein at least one of the internal signal pad and the peripheral
signal pad comprises a bonding pad.

20 3. The apparatus of claim 1 wherein at least one of the internal signal pad and the peripheral
signal pad has a buffer circuit associated therewith.

4. The apparatus of claim 1 wherein the internal signal pad is part of an area array of the
integrated circuit die.

25 5. The apparatus of claim 1 wherein the internal signal pad comprises an analog signal pad.

6. The apparatus of claim 1 wherein the switch is arranged nearer to the internal signal pad than to the peripheral signal pad.

5 7. The apparatus of claim 1 wherein the switch is arranged immediately adjacent to the internal signal pad, so as to minimize parasitic elements associated with the internal signal pad when the switch is in the first state.

10 8. The apparatus of claim 1 wherein the test access to the internal signal pad via the peripheral signal pad involves establishing electrical contact between an external probe and the peripheral signal pad.

9. The apparatus of claim 8 wherein the external probe comprises a test probe of a wire-type wafer probe card.

15 10. The apparatus of claim 1 wherein the switch is configured in the second state in conjunction with wafer-level testing of the integrated circuit die prior to separation of the die from a corresponding semiconductor wafer.

20 11. The apparatus of claim 1 wherein the integrated circuit die further comprises a control circuit configured to generate the control signal for controlling the state of the switch.

25 12. The apparatus of claim 11 wherein the control signal having one of the first and second signal characteristics comprises the control signal being at one of a first signal level and a second signal level, respectively.

13. The apparatus of claim 11 wherein the control circuit comprises at least one inverter, an output of the inverter being coupled to a control signal input of the switch.

14. The apparatus of claim 13 wherein the control circuit comprises first and second inverters connected in series, an output of the second inverter being coupled to a control signal input of the switch.

5 15. The apparatus of claim 13 wherein an input of the inverter is coupled via at least one resistor to a supply voltage terminal of the integrated circuit die.

16. The apparatus of claim 13 wherein an input of the inverter is coupled to an additional peripheral signal pad of the integrated circuit die.

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17. The apparatus of claim 1 wherein the integrated circuit die is packaged within a packaged integrated circuit.

18. The apparatus of claim 1 wherein the integrated circuit die is part of a semiconductor
15 wafer containing a plurality of dies.

19. A method of providing access to an internal signal pad of an integrated circuit die, the internal signal pad being arranged at a location away from a periphery of the die, the integrated circuit die further comprising a peripheral signal pad arranged proximate the periphery of the die and
20 a switch coupled between the internal signal pad and the peripheral signal pad, the switch being configurable in at least a first state in which the internal signal pad is not operatively connected to the peripheral signal pad, and a second state in which the internal signal pad is operatively connected to the peripheral signal pad, the switch being configurable in one of the first and second states responsive to a control signal having one of respective first and second signal characteristics, the
25 method comprising the steps of:

 configuring the switch in the first state during normal operation of the integrated circuit die; and

configuring the switch in the second state to permit test access to the internal signal pad via the peripheral signal pad.

20. A packaged integrated circuit comprising:

- 5 an integrated circuit die;
- a leadframe coupled to the die;
- the integrated circuit die and leadframe being at least partially enclosed by a packaging material;
- the integrated circuit die comprising an internal signal pad arranged at a location away
- 10 from a periphery of the die, a peripheral signal pad arranged proximate the periphery of the die, and a switch coupled between the internal signal pad and the peripheral signal pad;
- the switch being configurable in at least a first state in which the internal signal pad is not operatively connected to the peripheral signal pad, and a second state in which the internal signal pad is operatively connected to the peripheral signal pad;
- 15 the switch being configurable in one of the first and second states responsive to a control signal having one of first and second signal characteristics, respectively;
- wherein the switch is configured in the first state during normal operation of the integrated circuit die; and
- wherein the switch is configured in the second state to permit test access to the
- 20 internal signal pad via the peripheral signal pad.